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Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry

Presented by
The Massachusetts Semiconductor Coalition

Point of Contact:

Farhad Vazehgoo
Director , Advanced Technology Programs & Workforce Development
The MassTech Collaborative
75 North Drive, Westborough, MA 01581
Office: 508 870 0312 x479
vazehgoo@masstech.org

Preface

This response to your request for information entitled "Incentives, Infrastructure, and Research and Development Needs to Support a Strong Domestic Semiconductor Industry" is provided by *The Massachusetts Semiconductor Coalition*. The Commonwealth of Massachusetts, and the broader New England area, is home to a vibrant ecosystem of global semiconductor and technology leaders, universities, nonprofits and government organizations which include:

- Analog Devices
- Applied Material
- BAE Systems
- Draper Labs
- IQE
- MACOM
- MITRE Corporation
- Northeastern University
- Raytheon Technologies
- The Massachusetts Institute of Technology (MIT)
- The Massachusetts Institute of Technology – Lincoln Laboratory (MIT-LL)
- The Massachusetts Technology Collaborative (MassTech)
- UMass Lowell
- UMass Amherst
- Worcester Polytechnic Institute

Positions expressed in this response were developed in consultation with organizations across this New England semiconductor ecosystem. The views represented in this response are those of *The Massachusetts Semiconductor Coalition*, and not those of any particular organization listed above or with whom the coalition consulted. The views presented here were instead composed from, and represent an aggregate of, the diverse views expressed across the region.

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Introduction

The Massachusetts Semiconductor Coalition is pleased to provide inputs to the Department of Commerce's RFI. Our Coalition represents a growing group of companies, non-profit organizations, research institutes and universities that have come together with a particular focus on Intelligent and Secure Edge devices and applications. The emergence of future technologies such as AI, 5G/6G, new computing paradigms, and smart materials presents a strategic opportunity for the U.S. to get ahead of the next wave of devices and applications – including truly autonomous vehicles, next-generation communications, intelligent machines, integrated network systems-of-systems and digital healthcare - that will determine economic prosperity, national security, and our ability to address climate change and public health challenges.

Initially convened in May 2021 by the Massachusetts Technology Collaborative (MassTech), a quasi-public state agency, the Massachusetts Semiconductor Coalition has grown to include institutions and organizations that have operations beyond Massachusetts and impact that spans the globe. Indeed, members of the coalition include leading manufacturers of commercial analog/RF devices, major defense primes, critical suppliers of semiconductor equipment and materials, federally-funded research and development centers and world-class universities.

The Coalition members represent leading voices in the global semiconductor industry and many are communicating individual RFI responses to the Department, as well as providing inputs to responses from various industry associations. The Massachusetts Semiconductor Coalition response is intended to convey a particular viewpoint, shared by the coalition members, in which a collective effort emerges from the perspective and strengths of each individual entity.

It is the Coalition's position that Intelligent and Secure Edge devices and applications must be a key focus area for U.S. semiconductor investment. Leadership in this area is every bit as critical as advanced-node silicon based semiconductors as they are becoming ubiquitous from the front line of the battlefield to the shop floor of our factories. Devices that operate at the "Edge" of the digital and physical worlds transform our daily lives, the way businesses operate, how our armed forces protect our nation, and the impact we have on the world through a diverse set of applications such as smart phones, assisted driving, radar systems, factory automation and remote/wearable/implantable health care and diagnostics. These are the technologies that will continue to drive some of the most transformative changes in the world – 5G/6G, Industry 4.0, autonomous vehicles and mixed-reality (AR/VR). According to research firm IDC, more than half of global data volume in 2025 will be generated by Internet of Things (IoT) devices. Significant fractions of that data will be transmitted by advanced communication technologies, including 5G and 6G, to support the estimated 30 billion connected IoTdevices in 2025 [IoT-Analytics https://iot-analytics.com/state-of-the-iot-2020-12-billion-iot-connections-surpassing-non-iot-for-the-first-time/]. The U.S.

must assure that the underlying technologies that enable the collection and transmission of this data are robust, secure and resilient–we must control The Edge.

New England, along with other regions in the U.S., continues to be one of the world's leading centers of R&D in More Than Moore Technologies that rely on compound semiconductors, new materials development, system design and integration which will be critical to future leadership edge electronics. But that position is far from guaranteed. Other countries, including both close allies and more competitive nations have been very aggressive in investing in these critical areas – both in terms of manufacturing and R&D. We need a tightly-coupled innovate here, build here feedback loop. Today, the U.S. has no open-access, state-of-the-art R&D facility where companies and universities can drive development of next-generation edge device technologies, materials and fabrication equipment. This puts the U.S. innovation engine at a competitive disadvantage compared to other regions, where such facilities exist - Europe: LETI, imec, Fraunhofer; Singapore: IME; Japan: AIST; Taiwan: TSRI, ITRI and China – IMECAS (Beijing), SITRI (Shanghai) to name a few.

However, this is not solely a technology and manufacturing problem. The Coalition believes that it is critical to address the interrelated challenges presented by the technology, manufacturing, supply chain and workforce development required to overcome for Intelligent and Secure Edge devices and applications. Currently, the global semiconductor industry is made up of rather distinct ecosystems, aligned with various end-markets and applications. Technologies and facilities for leading-edge CMOS have limited relevance in the world of compound semiconductors. They rely on completely different materials sets (which are historically incompatible) and are manufactured at different scales (300mm for advanced-node electronics vs. 200mm, 150mm or 100mm for compound semiconductors). A critical gap exists in this landscape; the Coalition is focused on a gap in the nation's technology engine caused by lack of investment in, and broad access to, the non-silicon microelectronics technologies that will be foundational to the Intelligent and Secure Edge. It also builds the ecosystem needed to coordinate innovation at the intersection of materials, sensors, microelectronic devices, networks, software and applications at the scale currently only possible within the closed doors of the largest technology companies.

With that said, the future of microelectronics writ-large is the merging of these distinct ecosystems (e.g. leading-edge logic, memory, analog/RF) through a combination of heterogenous integration techniques, including advanced packaging and new monolithic processes. Leadership for the U.S. in microelectronics as a whole cannot be achieved without leadership in these 3 fundamental pillars, as well as the connective technologies of heterogenous integration that make them all possible.

New England's leading position in compound semiconductors and other new materials development and its unique combination of, and proximity to, the leading semiconductor, microelectronics, software and AI, life-sciences, defense, and robotics companies along with the best universities, hospitals and healthcare networks in the

world positions it as an ideal hub from which to drive key elements of the nation’s microelectronics strategy. Massachusetts in particular has a long track record of state-backed organization infrastructure in both deep tech innovation and advanced manufacturing. Building resiliency back into our semiconductor supply chain, reestablishing our technology leadership, and empowering our workforce of the future, is a defining moment for the nation. In doing so, we can cement United States’ leadership of the semiconductor industry and strengthen our critical supply chains, economy, and national security for generations to come.

Semiconductor Workforce

1. What are the greatest occupational or skills shortages facing employers in the semiconductor sector? What are the consequences of those shortages with respect to the domestic operation of employers in the sector? Considering all aspects of building, equipping, and running semiconductor manufacturing and R&D facilities, what actions have been taken to address these shortages, how effective have they been, and what gaps remain?

- Occupational/Skill shortage:
  - Science, Technology, Engineering and Math (STEM)-trained employees with a focus in the following areas: system engineering, electrical/electrnics engineering, mechanical/thermal, material science, physics, device physics, post-graduate researchers. For DoD use-cases staff need to be US persons and US citizens to meet export control requirements and security clearance eligibility.
  - Experienced electronics engineers with the expertise on the following areas:
    - System architecture, processors, algorithms, and simulation
    - RF, Monolithic Microwave Integrated Circuits (MMICs), analog, mixed-signal, rad-hard design
    - Advanced compound semiconductor device and design engineering
    - Digital Application Specific Integrated Circuit (ASIC) design (5nm to 14nm technology nodes, front-end system and logic design to back-end timing & layout, design-for-test)
    - Trusted & Assured Microelectronics (quantifiable assurance, provenance, authentication, traceability)
    - Microelectronics Cyber Security (hardware root-of-trust, design obfuscation, confidentiality and integrity protection, fault-tolerant designs)
    - Advanced packaging (2.5D, 3D heterogeneous integration, wafer-scale heterogeneous integration) engineers
    - Thermal/mechanical reliability engineering
    - Component engineering (test and verification)
  - Process development and integration engineers with the following expertise:
    - Material science, chemistry, chemical engineering, electrical engineering, industrial engineering
    - Semiconductor process and tool engineers
  - Packaging Engineers
  - Innovators to advance next generation military system research & development

        - New design architecture & partitioning (extreme heterogeneity, specialized accelerators, heterogeneous integration)
        - New devices and materials (TFETs, PETs, carbon nanotubes, graphene and other two-dimensional layered materials like transition metal dichalcogenides, spintronics)
        - New computational models (quantum, neuromorphic, approximate computing, dataflow)
        - Engineering leaders (e.g. Engineering and Management)
- Consequences:
    - The current workforce shortage is expected to impact a wide variety of applications and products, but it is especially concerning in military application-specific integrated circuits which require skilled analog, digital, RF, and mixed-signal IC designers experienced in both production and development including: RF and Deep-Submicron CMOS, FinFET, BiCMOS, SiGe, HV CMOS, SOI, GaAs, GaN, InP, HgCdTe, and other processes.
        - A shortage of qualified candidates to backfill normal workforce attrition will impact the ability to design and development next-generation microelectronics for DoD systems.
        - Aggressive strategies and measures are needed to address workforce shortages
            - To capture and transfer knowledge from an aging workforce.
            - To enable new technology disruptors for future computing, sensing, and communication appliances.
- Actions taken & effectiveness:
    - The industry has been trying to recruit, retain, and grow microelectronics design team for the last few years to advance microelectronics for DoD customers.
    - However, the global supply chain crisis beginning in 2020 to the present has directly (in our defense industrial base business segment) and indirectly (industrial, automotive, and consumer electronics business segments) tightened the availability of well-qualified candidates to support current and future microelectronics developments.

2. *What strategies have been most effective in addressing the shortages? Which states or countries have created the most effective strategies for different types of workforce needs to build, equip, and run semiconductor manufacturing and R&D facilities? What industry or other credentials do employers use, or could use, to train and hire workers to fill needed positions? To what extent do employers in the semiconductor sector partner with government institutions such as local workforce boards, economic development organizations, or Manufacturing Extension Partnership centers, or international partners*

to establish training and/or skill certification programs? To what extent do employers in the semiconductor sector partner with other employers to create joint training programs?

Current strategies have had very limited effectiveness in addressing the shortage. Programs exist which contain the right elements but unfortunately, for the most part, the programs are stand-alone "push" programs created by training/academic institutions in response to perceived needs. It is important to develop a more holistic approach:

- Step 1 is compiling a list of programs and attributes/features. This effort, if rigorously done, should identify areas of overlap and competition for resources. Alleviating competitive "pinch-points" should free up some resources to address other areas of need.

- Step 2 is engaging affected industry partners - Industry needs to provide the "pull" through detailing needs, providing funding, and guaranteeing employment to trainees.

- In parallel, a significant outreach effort needs to be done to increase the pipeline of K-12 students interested in microelectronics.

Which states or countries have created the most effective strategies for different types of workforce needs to build, equip, and run semiconductor manufacturing and R&D facilities?

South Korea – Adaptable Meister schools

Meister Schools are short to medium term efforts which address current workforce needs, as defined by affected industries. Since these are industry driven, they are also partially or fully industry funded.

Germany – Dual System (re: GOVET)

- Alignment between government, industry/labor, and academia
- Private funding from industry, complemented by Government funding
- National standards

What industry or other credentials do employers use, or could use, to train and hire workers to fill needed positions?

Referencing the German model, employers need to inform training/academic institutions of future needs in advance – this must be consistent with industry and national objectives. If the employer needs are specific, a dedicated program (re: Meister school) may be established.

To what extent do employers in the semiconductor sector partner with government institutions such as local workforce boards, economic development organizations, or Manufacturing Extension Partnership centers, or international partners to establish training and/or skill certification programs?

Limited extent – there are no national standards. As described previously, there are many excellent programs in existence, the overall effort falls short because there are few transitions from one program to the next. The limited (or no) coordination between existing programs also increases the overhead in each one of them, as each program has to find its own sponsors, industry partners, etc. In addition, there is almost no outreach effort to try to increase the pipeline of interested students in K-12. This is in clear contrast with the excellent K-12 outreach being performed by the software industry through initiatives such as "Hour of Code" and "Girls who code".

To what extent do employers in the semiconductor sector partner with other employers to create joint training programs?

Limited extent – current programs for specific employers are implemented to create a competitive advantage rather than benefit the industry as a whole. Additionally, these programs have been historically driven by today's needs and, as a result, have limited impact. Employers need to involve Career/Vocational Training Education (CTE/VTE) partners sooner (2 – 4 years) in parallel with strategic planning to create a collective and qualified pipeline where they can objectively draw from a pool of talent and subjectively deploy into their specific technology or industry.

3. What have been successful mechanisms used by employers in the semiconductor sector to work with local high schools, career and technical education programs, community colleges, or universities to recruit and train workers?

The shortage of skilled talent is forcing companies to try different strategies to develop their engineering and manufacturing workforce, however these efforts are typically at the local level and lack coordination with other companies.

Below are some examples of effort in this area:

Since 1998, many organizations like Analog Devices (ADI) manufacturing group have been working with the continuing education team at UMASS Lowell to offer onsite classes and certificate programs to help their own manufacturing employees broaden their skillsets by working towards associate and bachelor's degrees. Therefore, manufacturing employees with increased skills can now consider roles as process and equipment technicians, engineering, and supervisors. ADI's tuition reimbursement lessens the financial burden of paying for college classes while an ADI onsite program helps reduce the burden of logistics that takes pressure off "fitting one more thing" into their schedule.

In 2020, Analog Devices (ADI) Aerospace and Defense Group introduced a fellowship program with UMASS Lowell where engineers could earn a fully funded

master's degree while working part time and earning full salary. They developed this "home-grow your own talent" program for employees with US citizenship could easily pursue advanced engineering degrees that were needed for development work at ADI, which ultimately benefited the Department of Defense.

Analog Devices employs various advanced manufacturing roles, ranging from semiconductor to assembly and test manufacturing. Highly skilled operators ensure these tools are set up properly, performing efficiently, and producing zero defect quality. Advanced analytical tools are used to measure and analyze the inputs and outputs of the materials and processes. Since it is difficult to find highly skilled operators for these roles, it is important to provide an opportunity to train new-to-the-job-market workers, looking for second career workers, veteran workers, women, and other underrepresented minority workers. ADI has accepted this opportunity to grow a pipeline of new workers and train them with the experience needed for the electronics industry.

A key path to making this happen is partnering with local community college programs, such as the Microelectronics Bootcamp at Nashua NH Community College which provides students the training they need to be successful. The training focuses on military standards, microscope training, substrate attach, lean training, wire and ribbon bonding techniques, inspection, microelectronic manufacturing, resume building and die attach. These programs are designed to meet industry demands and teaches students basic military standards and assembly techniques for microwave electronic (MW) assemblies.

ADI recognizes the value of growing the pipeline of talent by tapping into STEM programs within local technical high schools. These partnerships are essential for the future of our business, developing next generation talent pools and growing a skilled workforce.

For example, the aerospace and defense manufacturing operations team at ADI works in partnership with local technical high schools, such as Shawsheen Valley Technical High School and Lowell Technical High School, to provide Co-op experiences as part of high school program requirements in their electronics and advanced manufacturing curriculum. Students gain real professional life experiences in technical and manufacturing roles while working in high tech environments and balancing a rotation of school.

From an academic perspective, UMASS Lowell piloted an early college certificate program where high school students can take 4 college courses, earn 12 credits, and receive an industry recognized credential before graduation. This initial program was in Manufacturing and began in 2018; there was a complementary program in Electronics scheduled to begin in 2020. Both programs have been dormant since the beginning of COVID but are expected to resume during the 2022 – 2023 academic year.

The Master's degree in electrical engineering is the preferred degree by the electronics and computer industries that have need for a highly-skilled and technical workforce. Historically, UMass Amherst's Electrical and Computer Engineering (ECE) Department has been the key school for BAE's and Raytheon's industrial education MS programs in microwave engineering covering topics across device, circuit and system levels including GaAS/GaN devices, RFIC/MMIC, and antennas and radar systems.

Employees from BAE and Raytheon complete the MSECE in three academic semesters taking eight courses synchronously with on-campus graduate students including hands-on labs courses using the most up-to-date microwave instruments. This course work is followed by six credits of on-site project work related to systems that BAE and Raytheon produce where each project is co-advised by a BAE/Raytheon engineer and a UMass ECE faculty member. Most recently the ECE department is expanding these workforce development programs to offer study in cloud computing, computer security, IoT and AI/ML systems

4. *Are there any current or planned initiatives in the semiconductor sector to strengthen and expand the recruitment of women and underrepresented minorities, including promotion of such careers at K–12 levels?*

Regionally, there are events which spotlight the state of the industry but, as described previously, they are not connected to other pathways. Also, as stated previously, many high school teachers do not know exactly what to teach for the semiconductor industry and further, since it is not connected to standards, there is no incentive to teach it. There is also very limited visibility of the microelectronics industry as a whole at the high school level.

It is important to create achievable, executable pathways for students to enter into semiconductors and electronics fields. These pathways for students and trainees should be achievable in a 6 – 18 months time frame between credentials/opportunities. The programs should also be "stackable" into degree pursuits.

To attract women and underrepresented groups, we need to highlight appropriate role models and emphasize the impact that these group have in the industry.

5*. To what extent, and for what occupations, do organizations in the semiconductor sector use the H1–B Program to fill positions?*

The current talent pool in US graduate programs in microelectronics is very heavily based on non US persons, and thus the microelectronics industry strongly relies on non US persons and on H1B visa candidates. In order to support the needs of the domestic microelectronics workforce, the US should incentivize this pool of candidates with permanent residency so that the pool of graduates can use their training in our domestic marketplace. If we are willing to teach them, then we should encourage them to stay vs exporting them.

6. *Are there opportunities to design the semiconductor incentive program to ensure that worker skills shortages do not hinder companies from expanding operations?*

It is critical that the semiconductor incentive program approaches workforce development in a holistic manner, as the industry is facing pervasive challenges to fulfill its current job openings. It is especially important to increase the pipeline of students interested in microelectronics by focusing on K-12. We need to work with K-12 educators to create teaching modules that highlight the impact of microelectronics in modern society, and its career paths to students. Industry/Government-sponsored electronic-focused high-school competitions could also increase the visibility of the entire industry among K-12 students. At the same time, new fellowship programs should be created to incentivise the study of microelectronics, in a way similar to how the current Reserve Officers' Training Corps (ROTC) program and the Stokes Educational Scholarship at the National Security Agency (NSA) programs attract new students into fields relevant to the military and NSA. Additional programs that will help to ensure a skilled workforce include:

- Summer internship programs that connect college students of all levels (from freshmen to PhD students) with industry. Freshmen and sophomore undergraduate students could especially benefit from these internships, as they are typically the students who find more difficulties in connecting with microelectronics companies and are also the students trying to decide what major to pursue in their studies.
- Co-Op programs that make internships in the microelectronics industry an integral part of the college degree.
- Vocational training programs in microelectronics.
- Professional education programs that allows both up-scaling and life-long learning in the industry.
- Outreach to ensure the broader society understand the impact of the microelectronics industry and connects with the people that make that happen.

Advanced Packaging Manufacturing Program

1. Please describe the application areas that are essential to long-term national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs. Examples include but are not limited to:

- *Analog device packaging*
- *Automotive*
- *Defense and aerospace*
- *Energy generation, transmission, conversion, and storage*
- *Harsh environments*
- *High performance computing, quantum computing, data centers*
- *Integrated photonics*
- *Integrated power electronics*
- *Internet of Things*
- *Mature packaging*
- *Medical, health & wearables*
- *MEMS and sensor electronics*
- *Mobile telecommunications*
- *Other?*

Advanced Packaging Manufacturing should be broadly defined. It should include leading-edge assembly and substrate technology (e.g. laminates, printed circuit boards and interposers) that have largely been off-shored to Asia. It should also include emerging packaging such as chiplets and 3D die stacking. Additionally, it should be broadened to include microsystems that include photonics, microfluidics, MEMS and other non-electronic components that will be used for various applications; some of which include bio-chem sensors in point-of-care medicine, hazardous gas detection / public safety, smart agriculture, robotics, and more.

There are two aspects to on-shoring leading-edge assembly and substrate technology. First is the need to provide cost-effective high-volume manufacturing for markets such as consumer electronics, 5G communication systems, and medical/industrial electronics. The second is the need to provide access to leading edge packaging technology for lower-volume verticals such automotive, defense and aerospace, and high-performance computing.

The Advanced Packaging Manufacturing should also include significant work to develop emerging and disruptive packaging technology for microsystems that are targeted at sophisticated sensing products. This includes 3D additive manufacturing techniques, micro-contact printing, heterogeneous integration, micro-embossing, and micro-injection molding.

Packaging technology will be increasingly used to combine disparate technologies manufactured on different wafer sizes or non-wafer form factors. The following application areas have overlapping packaging needs and should be grouped together:

- Defense and aerospace & Automotive & Harsh environments
- Defense and aerospace & Mobile telecommunications
- Photonics & Sensing & Medical, health, Wearables
- HPC & Integrated Power Electronics
- IoT solutions & sensors & signal processing & low-power & RF

2. Please describe the R&D core competencies that are essential to national leadership in semiconductor packaging, and, where possible, identify groupings where work must be closely coordinated in a program distributed in multiple hubs. Examples include but are not limited to:

- Alternative materials to mitigate impact of supply chain disruptions
- Artificial intelligence for design of packaging
- Assembly and test
- Emerging materials
- Heterogeneous integration, chip stacking, and related technologies.
- High-density substrates
- Metrology
- Modeling and simulation
- Package-level design/codesign tools for electrical, thermal and mechanical design of complex packages
- Printed circuit boards
- Safety and security
- Software, firmware, new concepts in programming
- Standards
- Test solutions to assure yield in complex packages
- Thermal solutions
- Other?
- Tooling

National leadership in advanced packaging requires a multi-pronged approach to R&D and require a broad set of capabilities.

- **Expand and extend Assembly and Packaging Capabilities:** It is necessary to on-shore existing assembly and packaging capabilities to establish the basis for industry-focused R&D, such as Laminates, Interposers, Bumping, and TSVs and

then expand and extend the technologies. This should be done in concert with investment in industry automation and modernization to be cost-competitive.
  - **Develop advanced Materials and Metrology:** Advanced materials are critical for national packaging leadership. This includes research in areas like thermal interface materials, laminate dielectrics, mold compounds, underfill materials, printable electronics inks (metal, dielectric, semiconductor) and more.
- **Advanced Assembly Techniques and Metrology:** Research on advanced assembly techniques such as embedded die, multi-die fanout, Wafer-to wafer, die-to-wafer, and die-to-die stacking is needed to support future 2.5 and 3D systems. This research will require advanced metrology and test techniques in order to enable and advance heterogeneous integration.
- **Non-conventional packaging:** Non-conventional packaging will be needed for many emerging applications such as biosensor, microfluidics, and photonics. The system solutions will require combinatorial innovation in bringing disparate technologies together.
- **Simulation**: Advanced packaging combines more components into a smaller space. Resulting detrimental effects such as heat dissipation, power and signal integrity issues need to be proactively analyzed and comprehended. This requires a focus on Chip-Package co-design tools and multi-physics simulation environments to evaluate and trouble-shoot the full system. Such simulation is required for the initial design of the full system, and needs to be optimized as the system is built and characterized.
- **Standards:** Development of standards (ideally open standards) related to packaging are key to enable a broad eco-system and leverage existing solutions. Chiplet interface standards, in particular, will play an important role here. To streamline a chiplet ecosystem development it is also critical to define and provide access to IP (library, curation, datasheets).
- **Security:** R&D capabilities in system security will be increasing relevant to mitigate counterfeiting and enable a “trusted” chiplet ecosystem.
- **AI and Machine Learning:** Many of the aspects above are dealing with increasingly complex systems. Artificial intelligence and Machine learning will likely be able to help in many of those aspects, such as new package designs, complex laminate layouts, material compositions or AI accelerators to simulate larger systems.

3. *A proposed National Advanced Packaging Manufacturing Program could be oriented to address multiple needs, including but not limited to prototyping, the provision of pilot lines, work force development, and supply chain development. Please describe the most critical needs on which the program should focus.*

The National Advanced Packaging Manufacturing Program should have an ecosystem that spans from discovery and innovation, through technology maturation and preproduction, to production. The current pipeline from discovery through

production is too long and difficult to transition the “Valley of Death”. Prototyping hubs and pilot lines are needed to accelerate and facilitate the transition from research to industry acceptance or pull. A NAPMP should support a broad set of technologies and applications.

1. On-shoring, evolving and advancing current technologies including advanced lithography, new materials, bumping, backend die finish, and substrates. Domestic-based advanced laminate suppliers are needed. The laminate supply chain should also address the raw materials sources. Facilities are needed to support chiplet-based systems is needed.
2. Exploring, developing and prototyping disruptive solutions for microsystems that include disparate novel technologies (i.e. micro-fluidics, MEMS, photonics, mechanical, bio, etc.) in addition to standard ICs.
3. Prototyping and access to on-shore packaging capabilities for low-volume applications based on advance packaging techniques used in high-volume applications. Government programs typically require low-volume access that are not always available on advanced packaging lines.

4. Create a national maker space (similar to Sematech or imec) that includes users, materials, process and equipment companies with sufficient funding to acquire new technologies to be used and tested by various users for different applications.

4. *What attributes are the most important for a National Advanced Packaging Manufacturing Program to deliver? Examples include but are not limited to:*

- ‘‘Leading edge’’ tools and modeling capabilities
- Characterization services
- Collaboration across multiple universities and multiple companies
- Development of education and workforce development infrastructure, including building a pipeline of skilled workers
- Easy to access facility, with different processes and tools
- Expert resident staff for custom development
- International participation
- Intellectual property protection for inventors
- Open access to intellectual property
- Post fabrication infrastructure
- Material investigation
- On-shore supply chain
- Other?

All factors listed are important for the NAPMP. Clarification on a few factors is provided below:

Accessibility to and support of a wide variety of tools, capabilities and technologies is of primary importance to accommodate the needs of a diversity of projects. Accessibility should also be provided to projects at various development stages and different volume size, i.e. a few wafers for prototyping and hundreds of wafers to assess technology maturity. The opportunity for researchers and developers to access and have "hands-on" experience is critical to **workforce development**.

Pre and post fabrication capabilities are essential. This includes modeling and simulations tools and support for design of packaged system. Metrology, test, failure analysis, and vulnerability assessment capabilities are also important.

International participation is desirable, however, it conflicts to some extent with domestic work force development goals. International participation could be considered beneficial if it expands process or IP offerings. It should also be considered if the use of NAPMP is paid for at reasonable rate.

On-shore supply chain, including substrate manufacturing, bonding, wafer processing, and TSVs is essential. In addition, maintaining strategic stores of critical materials to reduce dependency on foreign supply is vital to national security.

5. What factors are critical to enable a National Advanced Packaging Manufacturing Program to provide a successful packaging R&D hub(s)?

It is important to have clear top-down objectives that are tied to advancement/disruption of significant commercial verticals and/or national security. This should drive a significant fraction of the discovery and innovation programs as well as serve in the vetting at the technology maturation and preproduction transitions. Leading-edge packaging has existing roadmaps. Other advanced packaging technologies, such as advanced sensor microsystems, should similarly develop a vision based on market impact and guidance.

The packaging capabilities should leverage existing infrastructure and IP. Baseline process flow offerings should be made available, as well as leading edge tools to enable advancements over state-of-the art.

Partnership and funding opportunities between NAPMP, established industry and small start-ups including materials suppliers, tool vendors, and microelectronic entities will enable and accelerate a variety of packaging projects.

NAPMP Hubs should also focus on developing advanced packaging solutions using low cost and sustainable manufacturing such as additive manufacturing in addition to conventional technologies and developing and employing automation and AI/ML.

6. Identify processes, equipment, measurement capabilities, environmental conditions, and training facilities that are most crucial for facilities provided by a National Advanced Packaging Manufacturing Program. How might organizations access such facilities?

The ability to conduct R&D for packaging through experimentation with novel processes and structures, and with the ability for inspection and accurate measurements provided through metrology are needed for any advanced packaging programs. In respect to processes, the following capabilities are needed to be established or expanded to improve capacity:

- Drastically increase US-based package laminate/substrate fabrication (significant current gap)
- Backend wafer-level processes like bumping and wafer-thinning
    - The need to be support for wafer diameters ranging from 100-300mm
    - This will enable a wide range of technologies and materials, including III-V and wide bandgap (SiC, GaN) semiconductors which are important for power and RF applications
- Complex assembly services like flip chip
- Advanced over-molding like Film-Assisted-Molding and Strip-Grinding technology
- Conventional and high-density fanout technology down to 2 μm features
- Die-stacking and 3D system packaging techniques supporting μbumps and hybrid bonding
- Photonic package processes such as precision pick and place and additive optical interconnects
- Emerging package technologies for healthcare, biosensors (liquid or gas phase), MEMS, etc.
- Specialized package options for harsh environments and power products
- Promising additive manufacturing technology processes

In regard to characterization and test, the ability to inspect structures using optical, x-ray and acoustic methods of analysis are needed. In addition, evaluation of structures under harsh environmental conditions must be conducted with facilities and environmental chambers capable of supporting variations and extremes in: vacuum, temperature, humidity, thermal shock, radiation, and vibration. Furthermore, adequate test and reliability systems are needed to characterize advanced packages and complex systems (e.g. KDG capability for chiplets).

While instrumentation and measurement equipment along with environmental test chambers are expensive, particularly for state-of-the-art methods, academic labs may receive donations and may be equipped with leading edge R&D systems. Through cooperative agreements and financial support for operation of these facilities, government as well as commercial organizations, may be able to arrange access while also bolstering the knowledge base of future workers through stipends which keep the facility operating.

To accelerate the efforts for R&D and workforce development activities, it is important to make sure the affiliated organizations can easily access such facilities. One example for the operation of the shared facilities is the National Nanotechnology Infrastructure Network (https://www.nnin.org/) or its follow-on program (https://nnci.net/). Ideally, the following engagement models should be supported simultaneously at NAPMP:

1. Use facility directly through company employees for prototyping
2. Develop processes jointly between company and facility
3. Offered as a foundry service that both industry, universities and government organizations can access

7. How closely aligned should the capabilities enabled by a National Advanced Packaging Manufacturing Program be with those provided by the NSTC?

There should be close alignment between the National Advanced Packaging Manufacturing Program and the NSTC as advanced packaging is becoming an integral part of cutting-edge system solutions. NSTC made devices will need integration solutions to be developed by the NAPMP and that is most effectively accomplished done with shared, aligned roadmaps. Additionally, depending on the system, there are benefits to having all levels of the stack closely aligned in an ecosystem to allow for rapid feedback to accelerate innovation and optimization during development. It is important that the NAPMP and NSTC collaborate closely to achieve optimal integration and leverage the capabilities and needs of the NSTC. However, the NAPMP should be flexible and technology agnostic.

For the most advanced packaging technologies that require features like TSV's, hybrid bonding and silicon based active and passive interposers, development may occur at frontend sites. Aligning these requirements with post-fab packaging technology will be essential.

8. How should the National Advanced Packaging Manufacturing Program connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program?

There should be strong integration between the two programs since NSTC-made devices will need integration solutions to be developed by the National Advanced Packaging Manufacturing Program and that can only be done if they have combined roadmaps that comprehend the materials, device, processing, system architecture and packaging together. Overlap in the technology readiness levels

is expected since the NSTC output will be an input for National Advanced Packaging Manufacturing Program.

9. Describe anticipated needs in education and workforce development, including retraining and upskilling, in the semiconductor packaging area. How adequate is it currently, and what are future expectations of need? How should the workforce training pipeline be developed?

The proposed National Advanced Packaging Manufacturing Program and the National Network for Semiconductor R&D should have a strong education and workforce development in collaboration with colleges and universities. User facilities could be utilized for education and work development activities. Academic partnerships with universities would increase the visibility of advanced packaging and potentially draw in more universities.

To attract students' interest in the field of semiconductor packaging for workforce development, internship and co-op opportunities need to be provided. For training future R & D workforce, students with advanced degrees (PhD) in this field need to be recruited and trained. Currently, funding is lacking in this field to financially support enough PhD students and their research expenses.

University curriculum with a focus on semiconductor packaging needs to be developed. Such a concentration will involve related university programs on electrical engineering, mechanical engineering, and materials. Packaging focus classes and coursework within academia should be developed. Student interest and enrollment in semiconductor and VLSI classes offered by academia is already declining. The curriculum needs to be reinvigorated with a focus on microelectronics materials, device, process, and package.

To provide the proper support to achieve the above goals, investment in acquiring advanced equipment and simulation tools for educational purposes needs to be made at universities. Funding sources for hiring faculty and supporting PhD students needs to be established at the state and federal level. Coalition involving both industry and university partners will be initiated to provide timely training and job opportunities.

Onshore access and capability to start integrating new professionals in this area is needed. Having academia training in this area but no access or workforce opportunities onshore limits growth and pipeline development. Industry driven with academic and government alliances to support the workforce improvement and interests in the technology is essential. Deep information exchange between commercial and academia will help drive this development. This can be through workshops, lectures, student competitions, and networking with industry.

Semiconductor Financial Assistance Program

1. The term ''semiconductor'' is not specifically defined in Section 9902 of the NDAA; rather, the legislation leaves it to the Secretary of Commerce to define. What factors do you consider important in developing a definition of ''semiconductor'' for purposes of a semiconductor manufacturing incentives program?

- "Semiconductor" should be defined broadly. This should include all types of semiconductor and microfabricated integrated circuits that have significant commercial and/or national security impact. This broad definition includes leading-edge CMOS, trailing-edge CMOS, and CMOS for more specialized applications like high power, high voltage, radiation hardened, etc. It also includes compound semiconductor devices and wide bandgap semiconductor devices such as GaAs, GaN, InP, etc., that are used for electronic and optical applications. Low dimensionality electronic materials such as graphene, carbon nanotubes, and layered materials (e.g. transition metal dichachogenides) should also be considered. Beyond this, it should also include integrated photonic, micro-electro-mechanical (MEMS) devices and other non-semiconductor based microfabricated processes.
- "Semiconductor" should be defined to include the manufacturing ecosystem which supports the fabrication of the enumerated technologies including: chemicals and gases, mask-works creation, fabrication or processing equipment and clean room support materials.
- Finally, semiconductor should include facilities for advanced packaging heterogeneous integration and advanced microsystems to provide a higher-level of integration and utility for the fabrication "semiconductor" integrated circuits and realization as final products.

2. Section 9902 permits a ''consortium'' of public and private entities to apply for funding. What factors would public and private entities consider determining whether to apply for funding as part of consortium? How would private entities determine whether to work with a public entity as part of a consortium? How would a private entity consider working with other private entities (such as customers, equipment manufacturers, or capital providers) as part of a consortium?

Leading factors for determining consortium participation will include governance model that will be flexible to include companies of different sizes, an IP model that is broadly beneficial, open access to facilities and confidence that shared learning, contributions and support will accelerate innovation and provide positive differentiated outcomes.

3. *Based on the criteria outlined in Section 9902 of the NDAA, what types of facilities, equipment, and other capacity aligned with the manufacture of semiconductors do you see as being most critical to the interests of the United States?*

While leading node Si based CMOS technologies are important, mature Si nodes and other processes using alternative semiconductor materials are equally important to a

secure US supply chain. On-shoring these capabilities is crucial to our national defense and key markets in the U.S. that rely on semiconductor components for their end product or production (e.g. automotive). Note that these technologies can be on varied wafer diameters which is important consideration regarding equipment/tooling. While the US has a reasonable share of analog/special manufacturing today, we don't want to see that share shrink over the next 5 years due to the massive investments being made in China in the specialty nodes. Investments in a US-based packaging manufacturing facility (e.g. laminates) is needed to help level the playing field with the low cost Asian suppliers that are heavily subsidized by their governments.

4. *Based on the criteria outlined in Section 9902 of the NDAA, what do you see as presenting the biggest challenges for an organization to develop an application for funding as part of a consortium, and how long do you estimate it would take for an organization to prepare the required materials?*

One of the biggest challenges will be aligning on / understanding requirements for IP Sharing, including IP generated directly through program funding, IP generated by follow-on use of equipment and infrastructure built with government funding, and IP organizations share as in-kind contributions. This is less of a concern for pre-competitive research but becomes a greater barrier as development moves closer to commercial application.

Another is how shared access to facilities that receive government funding works. For both of these challenges, it will be important to set separate guidelines for funding targeting more collaborative research and development at universities, government, and non-profit organizations and funding whose primary goal is to incentivize private investment in domestic manufacturing.

5. *Subject to the criteria and eligibility requirements outlined in Section 9902 of the NDAA, what other factors should the Secretary consider as important when reviewing applications for Federal financial assistance?*

The DoC should consider the long-term commitment, sustainable business model, and viability of the recipient. Whether for an established consortium, firm or start-up in the sector, the entity should demonstrate the ability to leverage future investments and create a "flywheel effect."

The DoC should take into consideration the type of technology under request to ensure that the grants and NSTC funding are covering all parts of the semiconductor ecosystem while not spreading the funding so thin that it becomes ineffective.

6. *Section 9902 defines a covered entity to include, among other things public-private consortia, which could include partnerships between semiconductor firms and customers, suppliers, investors, state and local governments, federally funded research and development centers (FFRDCs), and other entities. How can Section 9902*

incentives be designed and deployed to encourage additional and new private capital investment in the semiconductor ecosystem? What can be learned from other technology infrastructure development programs that use such partnerships (e.g., data center facilities or communications infrastructure) that may be applicable to semiconductor facilities?

Incentives should target solutions of breakthrough challenges of critical importance to semiconductor industry segments. By creating an inclusive framework, private investors will see an opportunity to contribute and gain access to leading edge IP and expertise with the prospect of advancing existing segment or opening completely new technology segment.

7. *How can federal financial assistance, consortia, or public-private partnerships be structured to maximize the initial scale of projects and to ensure ongoing reinvestment in project expansions, tool upgrades, and productivity improvements for the projects to remain economically viable and competitive over time? What opportunities exist for manufacturers to partner with private capital providers or use project financing to maximize the impact of the Federal financial assistance awards to achieve these objectives?*

Funding through the CHIPS Act and FABS Act will only reflect a portion of the overall investment needed - the remainder will be through private enterprise, whether from the companies directly, through private financing, and at times through industry consortia. In advanced research, industry consortia can play a unique role in sharing equipment, facilities, and pre-competitive IP that ensures economic viability and maximizes the impact of federal funding.

8. *How can Federal funds incentivize the creation of a broad semiconductor ecosystem that includes producers of semiconductor manufacturing equipment and other upstream suppliers? What are the largest supply imbalances with respect to manufacturing equipment, tools, materials, and chemicals that need to be addressed by U.S. investment?*

No specific recommendations by the Massachusetts Semiconductor Coalition

9. *How can the program ensure that semiconductor startups and small and midsized companies have access to commercial fabrication, assembly, testing and packaging facilities and associated technical expertise, including intellectual property products such as "Process Design Kits"?*

To assure support to startups and small to mid-size companies, as a condition of manufacturing support:

1. All funded FAB organizations, as a condition of funding should commit to support an open Foundry model allowing access to supported technologies. Foundries who are truly open, supply as part of the business, PDK's to facilitate design and fabrication in a given Foundry.
2. The program should create a voucher system to subsidize the use of open Foundries for small businesses and startups. Preference in funding manufacturing infrastructure investment should be given to organization who offer foundry services as part of their normal, historic business practices. Any Company that is an actual open foundry will have the procedures in place to support the interaction from PDK through product qualification and packaging. Company to company interaction should be outside of the Government process and subject to mutually agreed commercial terms. If the Government has a desire to support startups and small businesses, funding could be supplied to facilitate foundry interactions.

10. *Under the law, the Secretary may consider whether a covered entity includes a small business concern as defined under Section 3 of the Small Business Act (15 U.S.C. 632). Would it be beneficial for the Department to encourage large entities to partner with medium and small business suppliers?*

To assure support to startups and small to mid-size companies, as a condition of Government manufacturing support:

3. All funded FAB organizations, should commit to a support an open Foundry model allowing access to Government supported technologies and infrastructure. Foundries who are truly open, supply as part of the business "Process Design Kits" as a routine element of the commercial foundry interaction.
4. It can be challenging for start-ups and small businesses to access Foundry processes due to the high economic barrier which exists in both the design and fabrication stage. To support small businesses, a potential solution for both phases is the creation a voucher system or direct support system to subsidize both the use of state-of-the-art EDA Toll and to access the Foundries, subsidizing standard mask costs and other requirements.
5. Preference in funding manufacturing and FAB infrastructure investment should be given to organizations who offer foundry services as part of their normal, historic business practices. Any Company that is an actual open foundry will have the procedures in place to support the interaction from PDK through product qualification and packaging. Company to company interaction should be outside of the Government process and subject to mutually agreed commercial terms. If the Government has a desire to support startups and small businesses, funding through voucher or other support mechanisms could be utilized to encourage and facilitate foundry interactions.

11. *Section 9902 requires a covered entity to make commitments to invest in workers and communities, including through training and education benefits and programs to expand employment opportunity for economically disadvantaged individuals. What constitutes a baseline commitment to worker training in the semiconductor industry and what other workforce investments should be considered? Are there international best practices or cooperation upon which your company finds beneficial? What other community investments should be considered beyond worker training and employment opportunities? How can worker training, other workforce commitments, and other community commitments be maximized and how should program participants be held accountable to their commitments? What types of programs exist, or could be expanded, to improve access for economically disadvantaged individuals to these workforce and community commitments and opportunities?*

No specific recommendations by the Massachusetts Semiconductor Coalition

12. *Section 9902 requires a covered entity to have secured commitments from regional educational and training entities and institutions of higher learning to provide workforce training to be eligible for funding. Looking at the semiconductor sector broadly, what are the greatest workforce development needs, and how can Federal financial assistance meet those needs? What specific types of workforce training programs would be the most beneficial to companies in these sectors? What existing workforce training programs have proven effective and should be expanded, including international exchanges or best practices? How could a program best ensure that workforce training and development meet critical national needs?*

Federal financial assistance can be effectively deployed to: 1) enhance current workforce development programs and 2) initiate new programs targeting the specific skill gaps the industry faces. Specific occupational and skill gaps have been identified as:

- Science, Technology, Engineering and Math trained persons in the following areas: system engineering, electrical engineering, mechanical/thermal, material science, physics, device physics,
- Experience and trained Integrated Circuit engineers with the expertise on the following areas:
    - System architecture, processors, algorithms, and simulation
    - RF, Monolithic Microwave Integrated Circuits (MMICs), analog, mixed-signal, rad-hard design
    - Advanced compound semiconductor device and design engineering
    - Digital Application Specific Integrated Circuit (ASIC) design, front-end system and logic design to back-end timing & layout, design-for-test)
    - Advanced packaging (2.5D, 3D heterogeneous integration, wafer-scale heterogeneous integration) engineers
    - Thermal/mechanical reliability engineering
    - Component engineering (test and verification)

- Semiconductor process development and integration engineers with the following expertise:
        - Material science, chemistry, chemical engineering, electrical engineering, industrial engineering
        - Semiconductor process and tool engineers
    - Packaging Engineers
- Trained Semiconductor Fabrication process technicians, test technician and assembly technicians
    - Foundational mathematics, chemistry, physics
    - Hands on virtual process equipment training
    - Hands on virtual test and characterization equipment training

To name a few. Federal funding to develop and enhance curricula and enhance program participation would directly strengthen the semiconductor manufacturing ecosystem in the U.S.

13. *What is the industry's environmental footprint in terms of its land and resource use, air quality and water quality impact, hazardous or other special-handling material needs, and greenhouse gas emissions impact? What is the industry currently planning or implementing on these dimensions and how will the environmental footprint likely change over the next decade as a result? What effect will semiconductor chip customers' "net zero" announcements or other related incentives have on the industry's environmental footprint? What opportunities exist for the industry to move to a smaller and more sustainable footprint, and how can such opportunities be used to create a stronger domestic market for chips produced with a smaller footprint?*

No specific recommendations by the Massachusetts Semiconductor Coalition

National Semiconductor Technology Center

1.Based on the functions outlined in section 9906(c) of the NDAA the Department's current vision of the NSTC is as a hub (or multiple hubs) of talent, knowledge, investment, equipment, and toolsets that tackles Moore's Law transitions, post-CMOS research into new materials, architectures, processes, devices, and applications, and that bridges the gap between R&D and commercialization. What attributes are most important for the NSTC to possess or provide to the community (e.g., ease of access, a broad suite of leading edge tools managed as central facility, a collaborative research environment)? What key factors are critical for the NSTC to address the current gaps in the semiconductor R&D ecosystem?

The future of microelectronics is the heterogeneous integration of different materials, devices, and circuits technologies at the device, wafer and package level. The NSTC should drive research and prototyping, with a path to production, across this full domain. To do so, leading-edge CMOS should be the central focus of the NSTC, but other semiconductor materials and processes will also be essential. The most significant threat to the US microelectronics industry and the downstream companies that depend on leading-edge CMOS ICs is slowed or stopped availability caused by off-shore production dependency that has been interrupted. Historically, companies that produce leading-edge CMOS invest substantial resources for in-house development to ensure the availability of technology for the next node on the CMOS roadmap.

The central question for the NSTC is how to enhance this process so that it has real benefit for US-based corporations producing leading-edge CMOS rather than simply duplicate this development and not have it onboarded into the production processes. With this in mind, it is important to have these leading-edge CMOS producers inform the needed research and development that is likely centered on technology needed for several nodes down the roadmap. To the extent that this is materials discovery and characterization, it may be appropriated to perform the research in an academic environment. However, development of novel devices at the leading edge will require access to tools that can produce the devices with appropriate dimensions and using production class tools. To the extent that cell library and low-level circuit design is needed to aid development of advanced capabilities, for example integrating memory into the back-end-of-line features, access to prototype fabrication of leading-edge nodes will be required.

The purview of the NSTC should also extend beyond leading-edge CMOS to include disruptive digital logic techniques, such as two-dimension material-based devices, superconductor-based circuits, and other approaches to reduce the power density that limits CMOS circuit performance. In addition to beyond-CMOS technology, the NSTC should investigate analog / mixed-signals circuits and the integration of CMOS and new materials. These include:

- Wide band gap IIIN such as GaN for next-generation high-power devices for RF and power grid / electric vehicle applications.

- III-V materials for integrated photonics at wavelengths other than the traditional 1.5 micrometer telecom band. Integrated photonics are becoming increasingly important for low-cost environmental mapping, lab-on-chip biosensors, quantum computing, and defense and national security systems.
- Novel oxides that would advance high Tc superconductors, ferroelectrics, etc.
- Heterogeneous integration of non-CMOS/more-than-Moore technologies along with leading-edge CMOS technologies to enable digitally-enhanced RF/analog and mixed-signal microsystems. This may include 3D wafer-scale and/or chiplet-based approaches to integrate diverse heterogeneous device technologies and interconnects.
- Additive manufacturing techniques that extend into the integrated circuit domain. Emerging techniques have the potential to use a variety of metal, dielectrics and semiconductors including 2D nanomaterials at nanometer resolution. These high-throughput techniques can create a new paradigm for a next generation of integrated circuits.
- Disruptive computing paradigms that radically alter power consumption for information processing and artificial intelligence. These include reversible, probabilistic, and brain-inspired/neuromorphic computing.

These disruptive microelectronics thrusts will not need the facilities of leading-edge CMOS. Thus, they could be developed at an innovation hub with 200-mm tools (or smaller depending on the technology) and an operating model that permits a wider range of materials into the fabrication facility. It is likely that there will be greater opportunity for academic engagement in these disruptive technologies as they are better aligned to the core academic research mission.

In all of these research thrusts, leading-edge CMOS, beyond leading-edge CMOS, and disruptive materials and microelectronics, the innovation hub has a critical function in creating the ecosystem that will speed transition from development to production. The hubs should onboard promising technology and speed their development by providing more sophisticated tools and deeper technical expertise. The hubs should also be in close coordination with the production constituents so that their needs are factored into which technologies to onboard and their early engagement in the technology maturation will speed the transition to production.

The hub facilities should also include activities centered on design, measurement, and engineering of the full-stack from devices through algorithms/applications. Next generation microelectronics will require co-optimization across traditionally stove piped elements of the technology. To achieve this, another important element for the hub facilities is space for collaboration, and shared design and simulation environments. This will help foster ideation and collaboration to accelerate the development to production path. This communication should include formal conferences, program reviews, and seminars; collaborative projects among

members at different points in the ecosystem; and informal brainstorming and chance discussions.

2. As authorized, the NSTC would have to be able to work with a wide range of research groups from industry, academia, and government, some of whom will be contributing valuable intellectual property. What approaches to intellectual property should be in place to protect the foundational contributions of members while enabling maximum collaboration and innovation amongst the research community supported by NSTC? What IP issues create unique challenges for middle- and late-stage prototyping collaborations versus early-stage research, design and proof-of-concept collaborations?

The NSTC should be charged with oversight of the IP licensing for technology created through this program. There is a balance to strike among the IP generation through the development process, the IP consumption through technology transition, and the US tax payer. The NSTC is in the unique position of wanting to encourage both IP generation and licensing, thus will be motivated to find an appropriate balance. Further, a primary goal of the NSTC is to give US-based production an economic advantage over foreign entities. Important IP should be protected by international patents and licensed at substantially higher rates, if at all.

3. The federal government has several programs that support microelectronics and associated R&D across many agencies, federal labs, university labs, corporate labs, and other for-profit and nonprofit entities. What existing domestic R&D activities, assets, intellectual property, knowledge and expertise should be incorporated or otherwise connected to the NSTC, and are any international in nature? How should the NSTC interface with federal labs, university labs, corporate labs and other existing institutions of R&D and prototyping to ensure that R&D projects are supported throughout the technology maturation process so that public research funds are able to improve R&D productivity and attract additional private and venture investment?

The NSTC should take advantage of existing facilities and infrastructure to a great extent. Building facilities from a “green field” is expensive, time consuming, and lacks existing expertise. The NSTC should make modest investments in tools and other infrastructure. However, most of the investments should be focused on performing the work of developing and maturing microelectronics (defined broadly) processes, design, testing, and demonstrations.

The funding and project activities should be coordinated to ensure rapid technology maturation. This coordination should include rigorous vetting at transition points where projects with strong indications of success receive adequate funding and access to appropriate equipment and expertise, and projects that do not pass the vetting are abandoned. Technology can enter this coordinated path at any point, given the current state of the technology. In the detailed description of this path below, it is assumed the technology is starting in a discovery phase that supported by other programs and funding mechanism that the NSTC will leverage.

- Robust portfolio of discovery and innovation projects with sufficient funding to perform competent and comprehensive exploration of emerging technology ideas. Since these activities will largely be performed within academia and national labs, they will also reinvigorate faculty and student enthusiasm for research in the microelectronics field and the increased number students, thereby contributing significantly to workforce development. A variety of discovery and innovation programs should be pursued including individual PI based programs and larger-scale collaborative programs centered on a bigger concept with participation from researchers in multiple institutions.
- Promising discoveries should be thoroughly vetted for their potential to have significant impact to the commercial and/or national security sectors. Technologies passing this vetting should be selected for aggressive technology maturation and likely transitioned into one of the technology maturation and preproduction facilities (hubs) that represent the NSTC. Here, additional expertise and more specialized tools can be used to accelerate technology maturation.
- If the technology still looks promising after technology maturation, it should undergo additional vetting and buy-in from the industrial partners in the ecosystem. This might include industry partners willing to transition the technology into their production. In such a preproduction phase, industry partners might tape-out into the process, augment the PDK or otherwise pursue advancements or differentiation for their offering of the technology.

4. How should the NSTC connect to National Network for Semiconductor R&D, authorized by Sec. 9903 of the FY 2021 NDAA? What considerations should be given to ensure strong integration between the two efforts? Should there be overlap in the technology readiness levels served by each program?

The National Network for Semiconductor R&D is intended to invest in immature or emerging technologies, primarily within the U.S. academic and government labs. There is a gap between these early stage investments and commercial viability where a VC or other commercial investments may move to mature these early stage to manufacturing stages. The NSTC should fill this gap, likely TRL 3 – 6, focusing their investments on applications of the early technologies and transition to manufacturing, with the National Network for Semiconductor R&D focusing on earlier stage research in the TRL 1-3 range. Industry generally is expected to invest in the transition from TRL 6 to 9. Clearly, there must be some overlap in funding across these transitions to ensure there are not gaps for promising technologies to mature as rapidly as possible.

5. How should the NSTC ensure that it can identify and invest in what comes next after the first wave of needs are identified in the initial years? To what extent does the semiconductor ecosystem need a long-term roadmap of application requirements, technical needs, and gaps in materials, tooling and equipment, and process capabilities in order to guide future R&D investments? How can the NSTC's investments best

support an open roadmap of this type, and how should the NSTC interface with other governments or allied international R&D programs, such as those established under Section 9905 of the FY2021 NDAA, to enable such a roadmap? What existing technology forums, roadmaps, or other initiatives should be incorporated into such efforts?

It is important to have top-down objective that are tied to advancement/disruption of significant commercial verticals (5G/6G/XG communications, Robotics/autonomous systems, digital healthcare, aerospace/defense, etc.) and/or national security impact. This should drive a significant fraction of the discovery and innovation programs as well as serve in the vetting at the technology maturation and preproduction transitions. Leading-edge CMOS has the IRDS roadmap. Other verticals should similarly develop a vision for market impact and guidance / roadmaps to achieve the desired impact. The responsibility for developing these visions/roadmaps should belong to the innovation hub personal, within their technology area expertise. These facilities are a natural nexus for the sub-ecosystems since the technology elements are on-boarded from the discovery and innovation institutions and transitioned out to the production taking place in industry.

6. The NSTC is envisioned as a public-private partnership. What are the most suitable models of public-private partnership for the R&D and prototyping gaps that the NSTC is envisioned to address? What are the roles of the public participants and the private-sector participants in this partnership, including any international participants? How should governance structures, program objectives, investment criteria, and oversight and accountability requirements be structured to maximize the transformative potential of the NSTC in the US R&D ecosystem?

The NSTC should adopt public-private partnership elements throughout the various aspects of its operation. There are multiple areas where this partnership is natural and beneficial. Several examples are given below:

- Facilities incorporated into the innovation hubs can be private and augmented with publicly funded tools and support for the personnel that operate the facility in performing the work of the NSTC.
- Innovation and early development-oriented projects that are performed in the innovation hubs can be supported with public funds, private funds or a combination of the two. Indeed, this should be a requirement of the hubs – allowing commercial entities to have access to the innovation hub facilities and personnel using their own funding. A final model relevant to the innovation phase is to provide vouchers for start-up companies that provides a portion of the funds for access to the innovation hub facilities. The State of Massachusetts has successfully implemented such a voucher system for start-up company access to university research infrastructure. Over the past four years nearly $6M has been granted to 227 companies through 682 vouchers.

- For technology transition-oriented programs, there is a natural opportunity for public-private partnership. Maturing integrated circuit fabrication processes can be 'run' in the innovation hub with access given to commercial companies looking to gain direct experience with the technology. The companies would support their own personnel cost, but the cost of the fabrication run would be cover through NSTC funding.
- The governance structures, program objectives, investment criteria, and oversight and accountability requirements could be structured similar to some of the advanced manufacturing institutes that worked well with industry and developed a friendly IP policy for industry and academia. Such structures have a governing council that includes the membership and decides on the investments and any major decision. Roadmaps are put together by the manufacturers, equipment developers, material suppliers, electronics users and research scientists from academia and government labs.

7. What operational and organizational characteristics, business processes, and practices will be important in ensuring that the resources of the NSTC are broadly accessible and available to the broader U.S. semiconductor R&D community including both small and larger, more established entities? How can the NSTC ensure that smaller and medium-sized companies and startups have access to facilities, expertise, and intellectual property that public funds support?

There are a couple of characteristics that should be implemented to achieve broad access to the NSTC hubs. First, the NSTC should consist of several hubs that are geographically diverse, ideally in areas with a higher concentration of microelectronics industry and academia. Even if the technology focus of the hubs is different in the various locations, having relatively easy access to hub personnel that can orient and assist the users access to the broader hub network facilities. Second, a significant portion of the hubs' capacity should be reserved for fee-for-access, thus eliminating the need for winning a government sponsored program to gain access. Finally, as mentioned above there should be several access models to the hubs' technology and infrastructure that will be better matched to the needs of large corporations and the needs of medium and small businesses. In the first case, the activities will be more technology transition focused. In the second case, the activities are more early development oriented.

8. For those who currently participate or have participated in a ''research consortium'' (either domestic or international) made up of public and private partners, what are the important lessons learned or best practices that the NSTC should follow?

There are two models of interest when considering the governance of the NSTC:

- The governance structures, program objectives, investment criteria, and oversight and accountability requirements could be structured similar to some of the

advanced manufacturing institutes that worked well with industry and developed a friendly IP policy for industry and academia. Such structures have a governing council that includes the membership and decides on the investments and any major decision. Roadmaps are put together by the manufacturers, equipment developers, material suppliers, electronics users and research scientists from academia and government labs.

- Another model is that of Sematech International and imec. The main reasons for the success of imec and the initial success and then collapse of Sematech is two factors; the first is continuous government funding which is essential for continuity (the US government stopped funding Sematech because they wanted to admit foreign companies and become an international consortium). imec still receive government funding (108 million euro per year 2017-2022). The second is that it is essential to include emerging technologies and research which Sematech did not do but imec did (with the exception of Sematch championing EUV lithography). Both Sematech and imec did adopt new processes and equipment and had teams from CMOS manufacturers, equipment vendors, and material suppliers on assignment working together on the new process development and scaling which worked out very well for Sematech and is still working well for imec.

9. What attributes or capabilities of the NSTC would make it attractive and beneficial for companies, universities, and other agencies to want to send employees for assignments at the NSTC? What types of research and training opportunities should be made available at the NSTC for students and early career staff?

The hubs within the NSTC should be welcoming and facilitated for robust collaborations. This is as critical a responsibility for the hub as providing access to tools and expertise. The role of the hub is to shape the microelectronics ecosystem. This starts by identifying the development opportunities that will have high economic impact, continues through design at the device, circuit and system levels, and finishes with fabrication and testing. There are multiple opportunities to have personnel and students assigned to an NSTC hub. These include:

- Hosting/funding internship/co-op and faculty/industry technical staff exchange programs
- Training students in the fabrication facility for careers as technicians and process engineers
- For early career staff, exposing them to the applications enabled by microelectronics innovations to accelerate their careers in semiconductors. Further, engaging them in early stage research will help prepare them to be the design and manufacturing leaders.
- Employees of companies, universities, and other agencies will benefit in multiple ways. First, through greater expertise in the specific objectives of their assignment, such as technology maturation, technology transition, or the system analysis skills to vet the impact of emerging technology. They will also

benefit from a better appreciation of the larger microelectronics ecosystem through the program reviews, seminars, and interactions with colleagues.

10. For organizations that currently utilize an external semiconductor "fab" as part of their R&D efforts, what services or processes are currently missing in the U.S. ecosystem that the NSTC should provide? Are there specific toolsets that the NSTC should own and operate or provide access to?

To create the next generation of microelectronics there will very likely need to be new materials, processes and tools developed to enable the truly heterogeneous solutions envisioned. The details of these needed will need to be defined with the research vision defined for the NSTC.

11. As authorized, the NSTC could establish an investment fund, in partnership with the private sector, to support startups and collaborations between startups, academia, established companies, and new ventures, with the goal of commercializing innovations that contribute to the domestic semiconductor ecosystem, including advanced metrology and characterization for leading-edge manufacturing processes, and for security and supply chain verification. How should this investment fund be structured, and what should be the roles of the public and private sectors in capitalizing, operating, and overseeing the fund and selecting its investment targets? Should the investment fund focus on early-stage investing, late-stage investing, or other stages of the process? How should the fund interact with existing private capital, both venture capital and established investment capital, and how can the fund sustain itself through its investments?

No specific recommendations by the Massachusetts Semiconductor Coalition.

12. How should the NSTC's investments and focus overlap or complement the investments and capabilities of foreign institutions such as the Interuniversity Microelectronics Center (imec) in Belgium or the French Laboratoire d'e´lectronique des technologies de l'information (CEALeti)?

The primary goal of the NSTC is to provide an economic competitive advantage for US-based companies and US-based microelectronics activities. IMEC or Leti do not have a mission to benefit US industry, thus there will be overlap and likely competition to get to market on development efforts with a high likelihood of economic impact. This includes developing a US-based supply chain to the greatest extent possible. However, there may be emerging technologies or yet unproven approaches that would benefit from collaborative and/or coordinated investments and development efforts.